1. APPLICATION

This specification manual applies to the conforming product specifications of the 68-pin, two piece FLASH EEPROM card of the JEIDA version 4.1 and PCMCIA version 2.0 associations.

2. FUNDAMENTAL CIRCUITS

2.1 MEMORY CAPACITIES

ITEM	MEMORY CAPACITY	MEMORY DEVICE CONFIGURATION
4-F-256	256 Kbyte	1 Mbit F-EEPROM x 2
4-F-512	512 Kbyte	2 Mbit F-EEPROM x 2
4-F-1M	1 Mbyte	2 Mbit F-EEPROM x 4
4-F-2M	2 Mbyte	2 Mbit F-EEPROM x 8
4-F-4M	4 Mbyte	2 Mbit F-EEPROM x 16

2.2 ERASE / PROGRAMMING CAPACITY

STANDARDS

ITEM	MIN	TYP	MAX	UNIT	(*NOTE*)
ERASE TIME		2 (1)	30	sec	(3)
WRITE TIME		4 (1)	25 (2)	sec	(4)
ERASE/ WRITE CYCLE	10,000	100,000			

NOTES:

1. 25 °C 12 V Vpp, 10,000 cycle measurement conditions.

2. During 400µ sec / BYTE, not including system overhead, the minimum block timing is 16µ sec.
(400µ sec / BYTE timing = 16µ sec x 25loop).
(16µ sec = 10µ sec BLOCK + 6µ sec byte recovery).
***Maximum CHIP programming timing has been expressed specifically slower than the slowest of the specifications above.
(Most of the byte programming timing is written faster than the byte programming worst cases.)

3. Does not include the programming timing (OOH) before erase.

4. Does not include system overhead time.

5. Attribute memory is an option available on FLASH memory cards. (see page 46 for attribute memory specifications).

3. CIRCUIT CONFIGURATION AND LOGIC

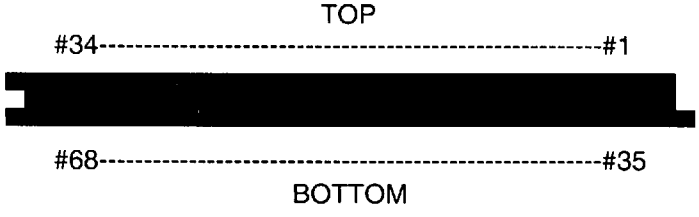
3.1 PIN ARRANGEMENT

PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG	PIN #	SIG
1	GND	11	A9	21	A12	31	D1	41	D15	51	Vcc	61	*REG
2	D3	12	A8	22	A7	32	D2	42	*CE2	52	Vpp2	62	*BVD2
3	D4	13	A13	23	A6	33	WP	43	NC	53	NC	63	*BVD1
4	D5	14	A14	24	A5	34	GND	44	NC	54	NC	64	D8
5	D6	15	*WE	25	A4	35	GND	45	NC	55	NC	65	D9
6	D7	16	NC	26	A3	36	*CD1	46	A17	56	NC	66	D10
7	*CE1	17	Vcc	27	A2	37	D11	47	A18	57	NC	67	*CD2
8	A10	18	Vppl	28	A1	38	D12	48	A19	58	RESET	68	GND
9	*OE	19	A16	29	A0	39	D13	49	A20	59	*WAIT		
10	A11	20	A15	30	D0	40	D14	50	A21	60	NC		

3.2 PIN DESCRIPTION

PIN #	DESCRIPTION
A0 ~ A21	ADDRESS INPUT
D0 ~ D15	DATA INPUT/OUPUT
*CE1, *CE2	CARD ENABLE
*OE	OUTPUT ENABLE
*WE	WRITE ENABLE/PROGRAM
Vpp1, Vpp2	PROGRAM SUPPLY VOLTAGE
*CD1, *CD2	CARD DETECT
*BVD1, *BVD2	BATTERY VOLTAGE DETECT
WP	WRITE PROTECT
*REG	REGISTER SELECT
RESET	RESET
*WAIT	WAIT
Vcc	POWER (+5V)
GND	GROUND
NC	NO CONNECTION

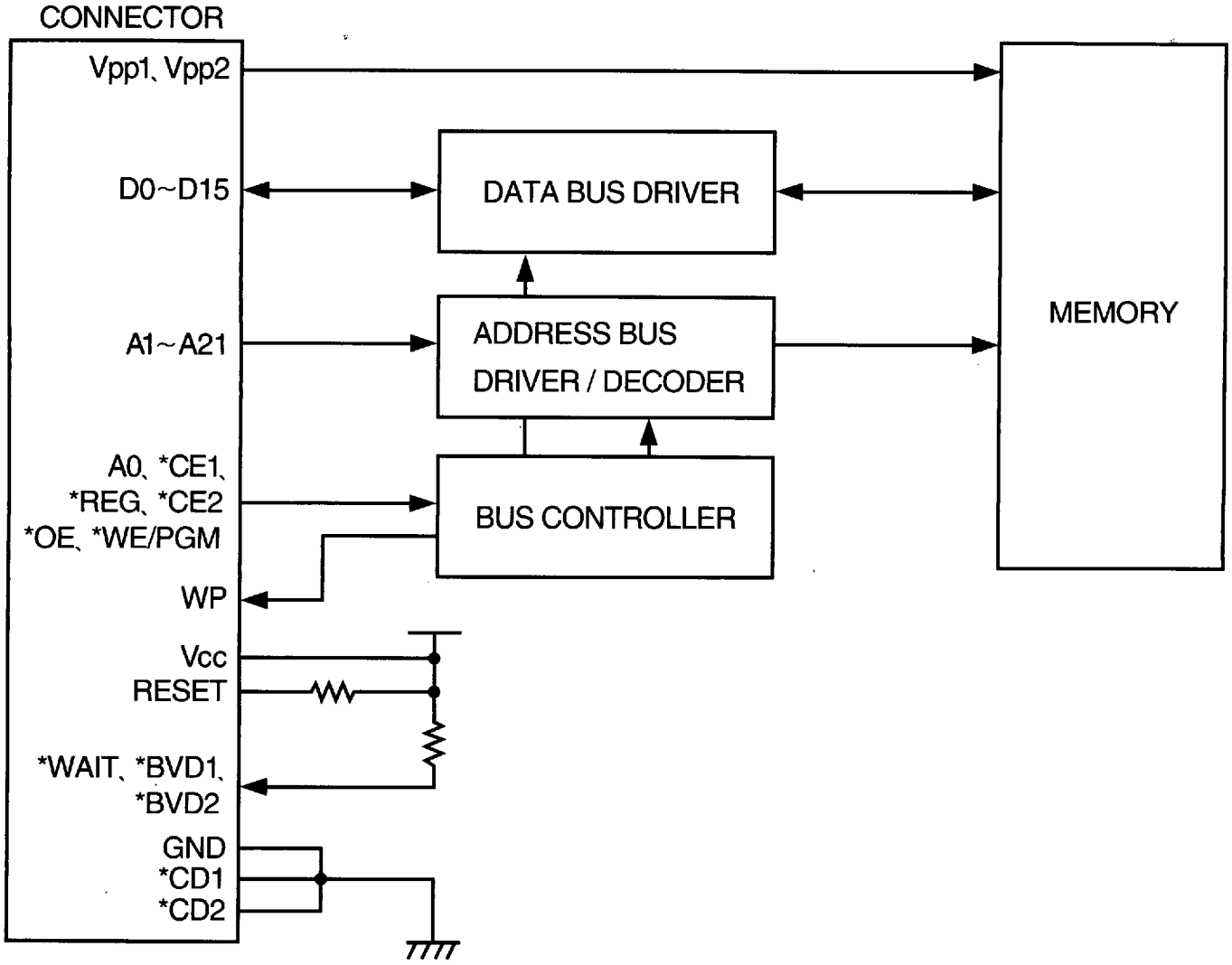
3.3 PIN DIAGRAM



NOTES:

1. This PIN arrangement conforms with the standards set by JEIDA 4.1/PCMCIA 2.0.
2. *256 Kbyte....PIN #48, 49, 50 are Not Connected.
   *512 Kbyte....PIN #48, 49, 50 are Not Connected.
   *1 Mbyte.....PIN #49, 50, are Not Connected.
   *2 Mbyte.....PIN #50 is Not Connected.

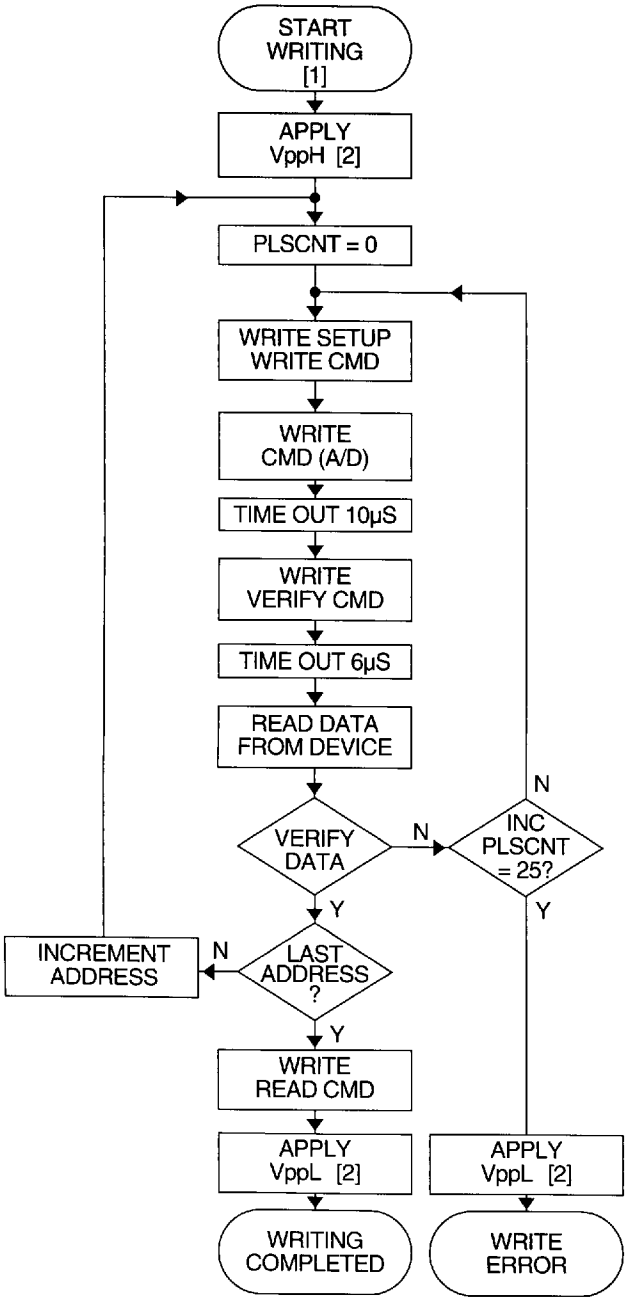
3.4 BLOCK DIAGRAM



NOTES:

1. *RESET = 100KΩ pull-up
2. *BVD1, *BVD2, *WAIT = 100KΩ pull-up

3.5 BYTE * PROGRAMMING FLOW CHART

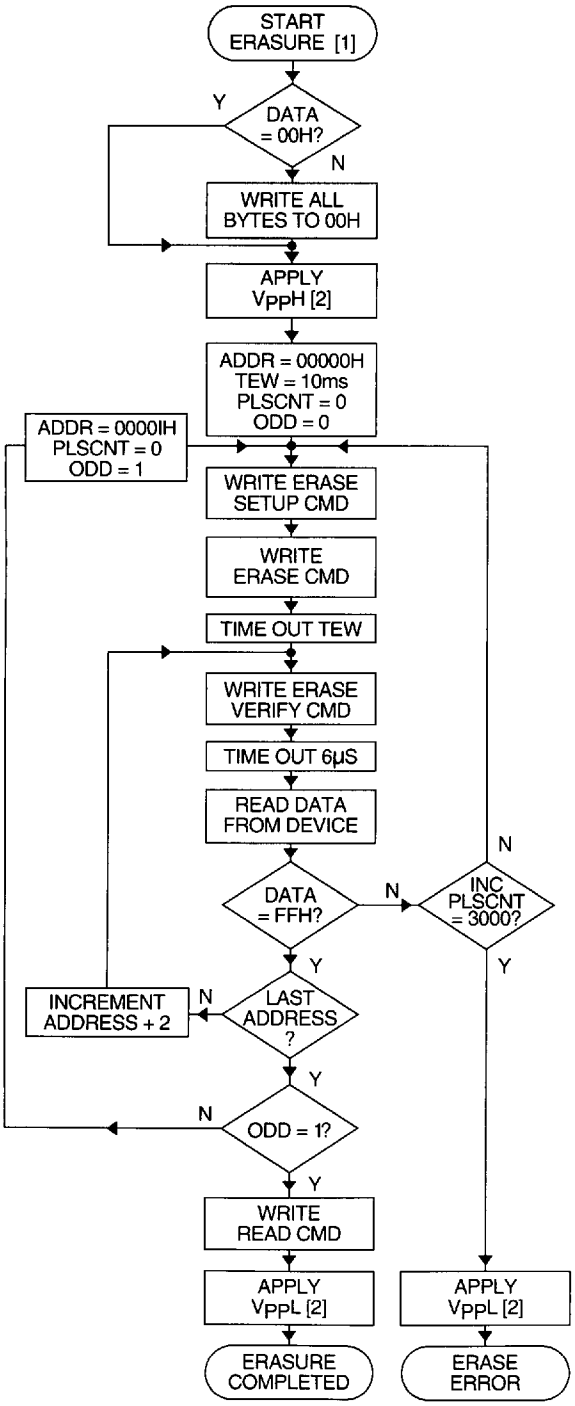


BUS OPERATION	COMMAND	COMMENTS
STANDBY		Wait for V_{PP} ramp to $V_{PP}H$ (=12,0 V) [2] Initialize pulse-count
WRITE	Setup Write	Data = 40H
WRITE	Write	Valid address/data
STANDBY	[3]	Duration of Write operation (t_{WHWH1})
WRITE	Write Verify	Data = C0H; stops Write Operation [4]
STANDBY		t_{WHCL}
READ		Read byte to verify Write Operation
STANDBY		Compare data output to data expected
WRITE		Data = 00H, resets the register for read operations
STANDBY	Read	Wait for V_{PP} ramp to $V_{PP}H$ [2]

NOTES:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of VppH and VppL.
3. Write Verify is only performed after a byte write operation. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

3.6 BYTE * ERASE FLOW CHART



BUS OPERATION	COMMAND	COMMENTS
STANDBY		Wait for V_{PP} ramp to $V_{PP}H$ (=12,0V) [2] Use Write Operation Algorithm Initialize even/odd addresses, erase pulse width, and pulse count
WRITE	Setup Erase	Data = 20H
WRITE	Erase	Data = 20H
STANDBY		Duration of Erase operation (t_{WHWH2})
WRITE	Erase Verify [3]	Addr = Byte to verify; Data = A 0 H; Stops
STANDBY		Erase Operation [4] t_{WHOL}
READ		Read byte to verify erasure
STANDBY		Compare output to FFH increment pulse count
WRITE	Read	Data = 00 H, resets the register for read operations
STANDBY		Wait for V_{PP} ramp to $V_{PP}L$ [2]

NOTES:

1. CAUTION: The algorithm MUST BE FOLLOWED to ensure proper and reliable operation of the device.
2. See DC Characteristics for the value of VppH and VppL.
3. Erase Verify is only performed after chip erasure. A final read/compare may be performed (optional) after the register is written with the Read command.
4. Refer to principles of operation.

3.7 DATA BUS OPERATION

READ ONLY

OPERATION MODE	Vpp2	Vpp1	*CE2	*CE1	A0	*OE	*WE	D8-DI5	D0-D7
READ (x 8)	VppL	VppL	H	L	L	L	H	HIGH-Z	O/P EVEN-BYTE
READ (x 8)	VppL	VppL	H	L	H	L	H	HIGH-Z	O/P ODD-BYTE
READ (x 8)	VppL	VppL	L	H	X	L	H	O/P ODD-BYTE	HIGH-Z
READ (x 16)	VppL	VppL	L	L	X	L	H	O/P ODD-BYTE	O/P EVEN-BYTE
OUTPUT dis	VppL	VppL	X	X	X	H	H	HIGH-Z	HIGH-Z
Non SELECTED	VppL	VppL	H	H	X	X	X	HIGH-Z	HIGH-Z

READ/ WRITE

OPERATION MODE	Vpp2	Vpp1	*CE2	*CE1	A0	*OE	*WE	D8-DI5	D0-D7
READ (x 8)	VppX	VppH	H	L	L	L	H	HIGH-Z	O/P EVEN-BYTE
READ (x 8)	VppH	VppX	H	L	H	L	H	HIGH-Z	O/P ODD-BYTE
READ (x 8)	VppH	VppX	L	H	X	L	H	O/P ODD-BYTE	HIGH-Z
READ (x 16)	VppH	VppH	L	L	X	L	H	O/P	O/P
WRITE (x 8)	VppX	VppH	H	L	L	H	H	HIGH-Z	I/P EVEN-BYTE
WRITE (x 8)	VppH	VppX	H	L	H	H	L	HIGH-Z	I/P ODD-BYTE
WRITE (x 8)	VppH	VppX	L	H	X	H	L	I/P ODD-BYTE	HIGH-Z
WRITE (x 16)	VppH	VppH	L	L	X	H	L	I/P ODD-BYTE	I/P EVEN-BYTE
Non SELECTED	VppH	VppH	H	H	X	X	X	HIGH-Z	HIGH-Z
OUTPUT dis	VppH	VppH	X	X	X	H	H	HIGH-Z	HIGH-Z

"H" = Vih, "L" = Vil, "X" = DON'T CARE "H" or "L" = "VppH or VppL"

"VppH" "VppL", VppX = DON'T CARE "H" or "L"

NOTE:

WP (WRITE PROTECT): When in "H", Write is not possible.

3.8 COMMAND REGISTER DEFINITIONS

BUS MODE	COMMAND	NECESSARY BUS CYCLE	FIRST BUS CYCLE			SECOND BUS CYCLE		
			OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA
BYTE MODE	MEMORY READ	1	WRITE	X	00H			
	SETUP ERASE /ERASE	2	WRITE	X	20H	WRITE	X	20H
	ERASE-VERIFY	2	WRITE	EA	A0H	READ	X	EVD
	SETUP PROGRAM /PROGRAM	2	WRITE	X	40H	WRITE	PA	PD
	PROGRAM-VERIFY	2	WRITE	X	C0H	READ	X	PVD
	RESET	2	WRITE	X	FFH	WRITE	X	FFH
WORD MODE	MEMORY READ	1	WRITE	X	0000H			
	SETUP ERASE /ERASE	2	WRITE	X	2020H	WRITE	X	2020H
	ERASE-VERIFY	2	WRITE	EA	A0A0H	READ	X	EVD
	SETUP PROGRAM /PROGRAM	2	WRITE	X	4040H	WRITE	PA	PD
	PROGRAM-VERIFY	2	WRITE	X	C0C0H	READ	X	PVD
	RESET	2	WRITE	X	FFFFH	WRITE	X	FFFFH

NOTES:

1. EA = Address of memory read during Erase-Verify.
PA = Address of memory read during Program-Verify.
ECD = Data read from the EA address during Erase-Verify.
PD = Data programmed by the PA address.
PVD = Data read from the PA address during Program-Verify.

2. Read/Write operation: Vpp1 = Vpp2 = VppH = 12V TYP.

3. Flow Chart for Byte operation is shown in 3.4 & 3.5.

4. ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	SIGNAL	RATING	UNIT
SUPPLY VOLTAGE	Vcc	-0.5~+6.0	V
INPUT VOLTAGE	Vin	-0.5~Vcc+0.5	V
OUTPUT VOLTAGE	Vout	-0.5~Vcc+0.5	V
PROGRAM VOLTAGE	Vpp (1/2)	-0.5~+13.5	V
OPERATION TEMPERATURE	Topr	0~+60	°C
STORAGE TEMPERATURE	Tstg	-20~+70	°C

5. RECOMMENDED OPERATING CONDITIONS

SIGNAL	DESCRIPTION	RATING		UNIT
		MIN	MAX	
Vcc	SUPPLY VOLTAGE	4.75	5.25	V
Vpp (1/2)	Vpp 1/2 HIGH VOLTAGE("H" LEVEL)	11.40	12.60	V
	Vpp 1/2 LOW VOLTAGE("L" LEVEL)	0.00	Vcc+2.0	V
VIH	INPUT VOLTAGE "H" LEVEL	2.4		V
VIL	INPUT VOLTAGE "L" LEVEL		0.8	V
Topr	OPERATING TEMPERATURE	0	+55	°C

6. ELECTRICAL CHARACTERISTICS

6.1 DC CHARACTERISTICS

SIGNAL	DESCRIPTION	RATING		UNIT	*NOTE
		MIN	MAX		
I LI	INPUT LEAK CURRENT (OTHER THAN *CE, *WE)	-10	10	µA	1
	*CE, *WE	-560	10	µA	2
I LO	OUTPUT LEAK CURRENT	-10	10	µA	2
I SB	STANDBY CURRENT		5	mA	4
I CC1	OPERATION CURRENT		65	mA	5
I CC2	HALF OPERATION CURRENT		100	mA	6
I IH	INPUT VOLTAGE "H" LEVEL	2.4		V	
I IL	INPUT VOLTAGE "L" LEVEL		0.8	V	
I OH	OUTPUT VOLTAGE "H" LEVEL	3.8		V	7
I OL	OUTPUT VOLTAGE "L" LEVEL		0.4	V	8

NOTES:

1. V IN = 0~Vcc, without *CE, *WE or *REG
2. V IN = 0~Vcc
3. V out = 0~Vcc, *CE1 and *CE2 = V IN *CE = V IH or *WE = V IL
4. *CE ≥ Vcc -0.2V
5. *CE = V IL, V IN = V IH or V IL, I out = 0mA
6. Cycle = MIN, Duty =100%, I out = 0mA
7. I OH = -2.0mA
8. I OL = 3.2mA

6.2 AC CHARACTERISTICS

READ & VERIFY CYCLES

SIGNAL	DESCRIPTION	RATING		UNIT
		MIN	MAX	
$t_c(R)$	READ CYCLE TIME	200		ns
$t_a(A)$	ADDRESS ACCESS TIME		200	ns
t_{CE}	CHIP ENABLE ACCESS TIME		200	ns
t_{OE}	OUTPUT ENABLE ACCESS TIME		100	ns
t_{OH}	OUTPUT HOLD FROM ADDRESS, CE OR OE CHANGED (*1)	30		ns
t_{LZ}	CHIP ENABLE TO OUTPUT IN LOW – Z	5		ns
t_{OLZ}	OUTPUT ENABLE TO OUTPUT IN LOW – Z	5		ns
t_{EHQZ}	CHIP DISABLE TO OUTPUT IN HIGH – Z		90	ns
t_{DF}	OUTPUT DISABLE TO OUTPUT IN HIGH – Z		90	ns
t_{WHGL}	WRITE RECOVERY BEFORE READ	6		ns

NOTE:

*1. Whichever comes first.

WRITE/ ERASE/ PROGRAM CYCLES

SIGNAL	DESCRIPTION	RATING		UNIT
		MIN	MAX	
t_cW	WRITE CYCLE TIME	250		ns
t_{AH}	ADDRESS HOLD TIME	180		ns
t_{CH}	CHIP ENABLE HOLD TIME	0		ns
t_{DS}	DATA SETUP TIME	80		ns
t_{DH}	DATA HOLD TIME	50		ns
t_{WP}	WRITE PULSE WIDTH HIGH	150		ns
t_{AS}	ADDRESS SETUP TIME	30		ns
t_{WHGL}	WRITE RECOVERY TIME BEFORE READ	6		ns
t_{GHWL}	READ RECOVERY TIME BEFORE WRITE	0		ns
t_{CS}	CHIP ENABLE SETUP TIME BEFORE WRITE	20		ns
t_{WPH}	WRITE PULSE WIDTH HIGH	20		ns
t_{WHWH1}	DURATION OF PROGRAMMING OPERATION	10		ns
t_{WHWH2}	DURATION OF ERASE OPERATION	9.5		ns
t_{VPEL}	VPP SETUP TIME TO CHIP ENABLE LOW	1.0		ns

Vcc=5V±5%, Vpp=12V±5%, Topr=0~50°C

NOTES:

1. Read timing characteristics during Read/Write operations are the same as during Read-only operations. Refer to AC characteristics for Read-only operations.

2. Rise/Fall time ≤10ns.

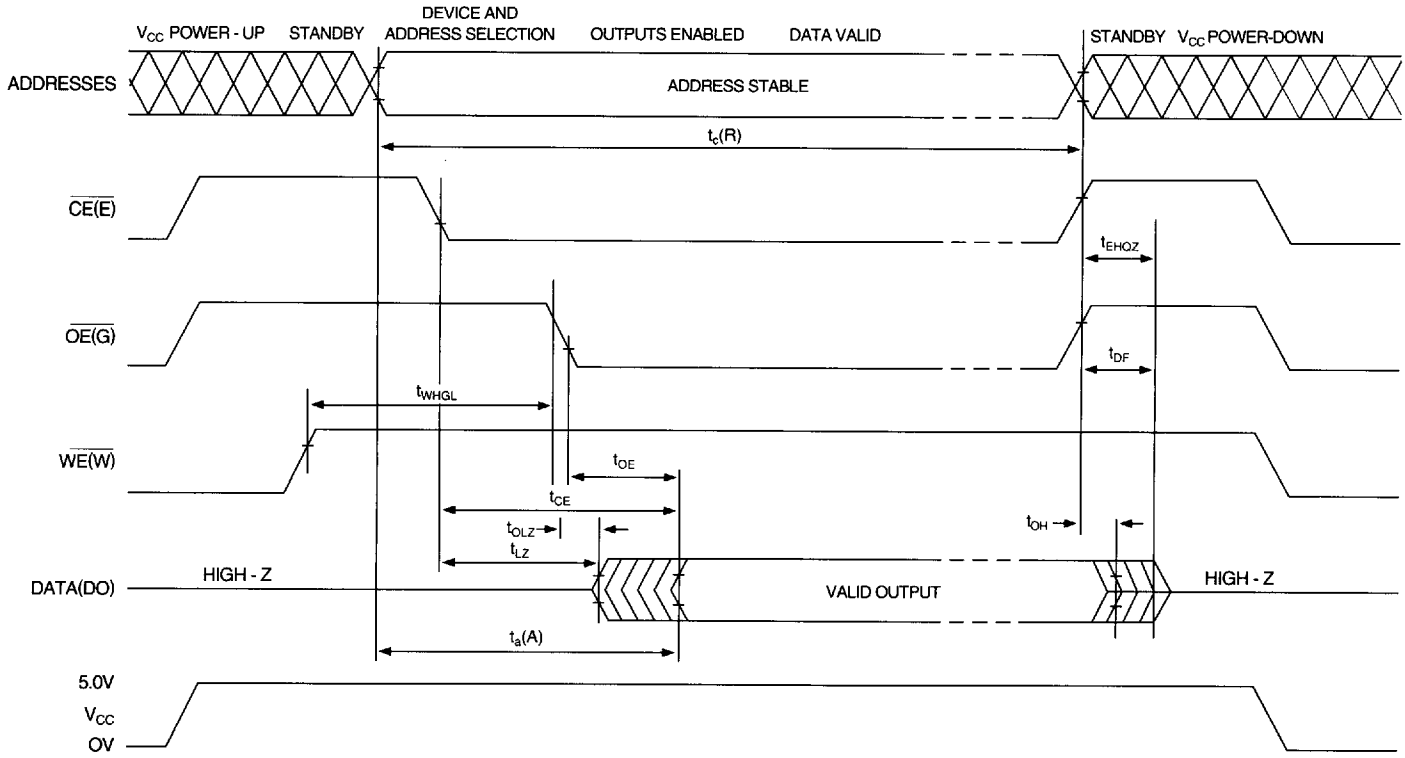
3. The integrated stop timer terminates the programming/erase operations, thereby eliminating the need for a MAX specification.

6.3 TERMINAL CAPACITANCE

ITEM	CONDITION	SIGNAL	MIN	MAX	UNIT
INPUT TERMINAL	f=1MHz	C IN		35	pF
OUTPUT TERMINAL	T opr=25°C	C OUT		35	pF
INPUT/OUTPUT TERMINAL	V i/o = OV	C I/O		45	pF

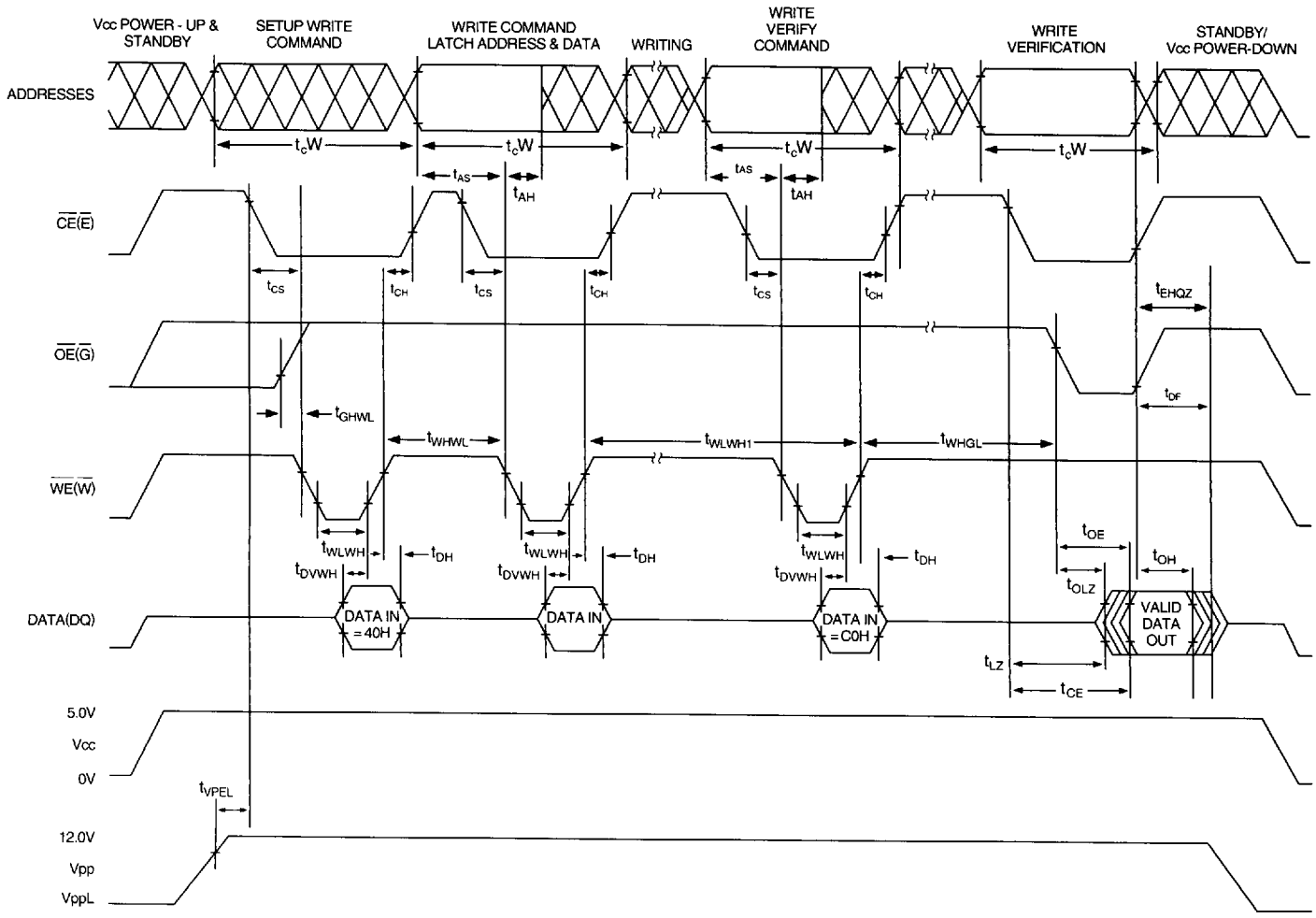
7. TIMING DIAGRAMS

7.1 READ CYCLE



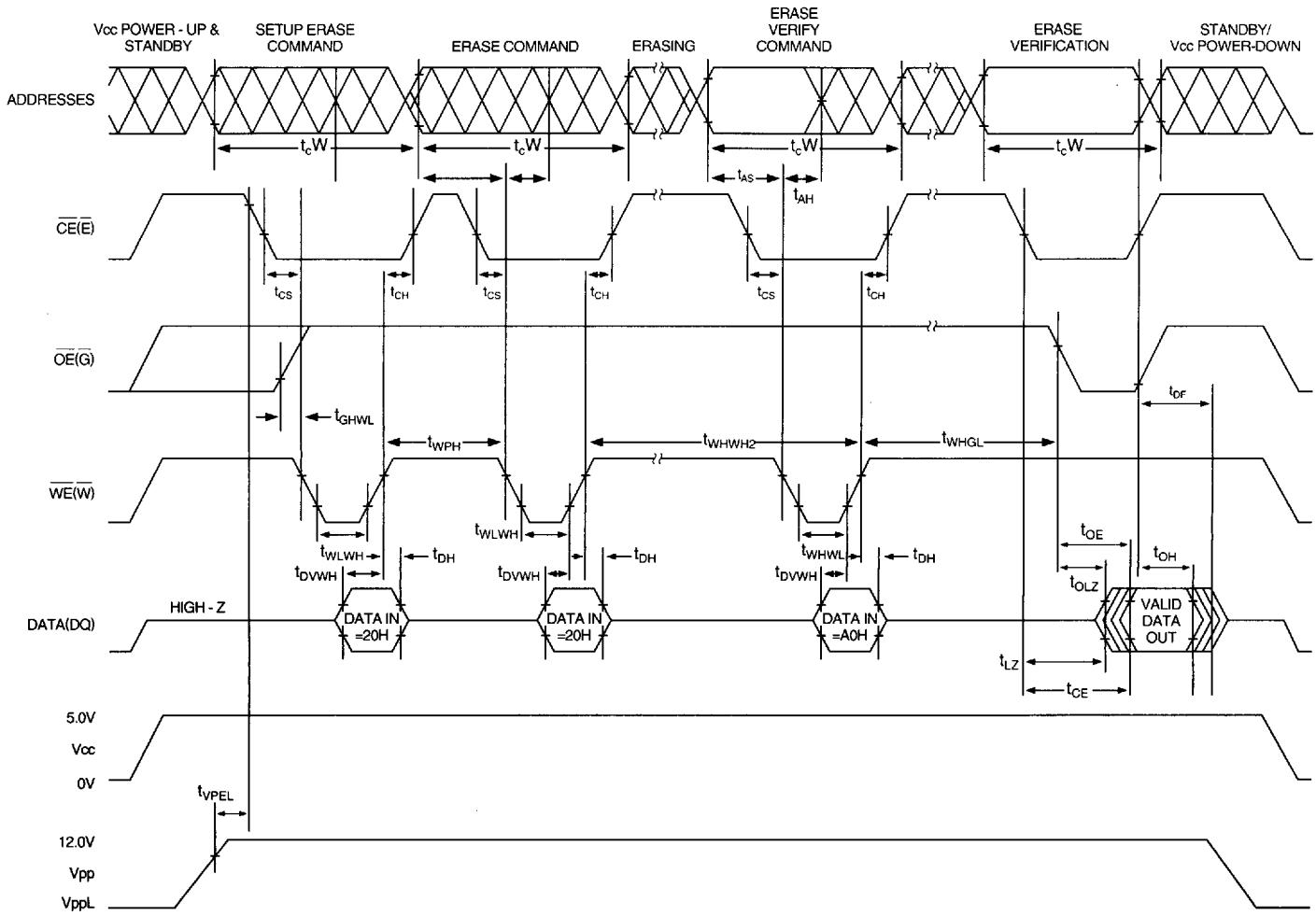
NOTE:
$\overline{CE}$ refers to $\overline{CE}_{1,2}$

7.3 PROGRAMMING CYCLE



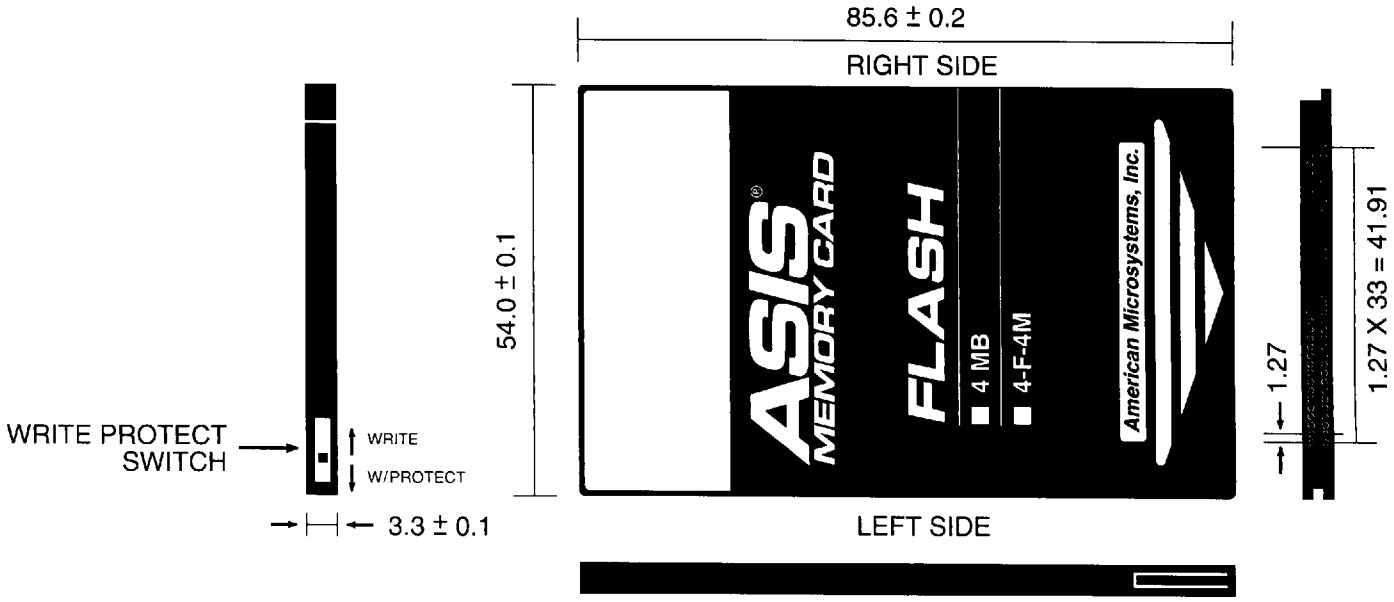
NOTE:
$\overline{CE}$ refers to $\overline{CE}_{1,2}$

7.4 ERASE CYCLE



8. MECHANICAL CHARACTERISTICS

8.1 EXTERNAL DIMENSIONS



9. CARD INSPECTION

9.1 SPECIAL FEATURE TESTING

#	ITEM	TESTING PARAMETERS	TEST TEMPERATURE	# INSPECTED
1	High Temperature Operation	Read/Write, Data Retention, Battery conditions are +5.25V / +4.75V.	+55°C	All
2	External Examination	Correct markings, correct labeling, no marks or scratches, WP switch is in WRITE position.	Room Temperature	All